REMARKS

In view of the above amendments and the following remarks, reconsideration and further examination are requested.

Claims 6 and 13 were objected to for failing to further limit the claims. Claims 6 and 13 are canceled herein.

Claim 3 has been rewritten in independent form to include the limitations of claim 20, claim 9 has been rewritten in independent form to include the limitations of claim 23, and claim 16 has been rewritten in independent form to include the limitations of claims 23 and 12.

Claims 1, 2, 5-8, 12-15, 20, and 23 have been canceled. Therefore, claims 3, 4, 9-11, 16-19, 21, 22, and 24-27 are pending.

Claims 2-4, and 6-27 were rejected under 35 U.S.C. § 102(e) as being anticipated by Lasserre (US 6,760,829). This rejection is traversed and is inapplicable to claims 3, 4, 9-11, 16-19, 21, 22, and 24-27 for the following reasons.

Claim 3 recites a processor connected to a memory via a data bus, the data bus having a data width, said processor being a second-endian type processor which is usable with a first-endian type processor. Claim 3 recites the following features (A)-(C), with feature (C) including features (C1)-(C3). Specifically, claim 3 recites that the processor comprises:

(A) a processor bus logically connected to the data bus in a first-endian order;

(B) an address conversion unit operable to perform an address conversion on at least one lower bit of an address so as to indicate a reversed position of data in the data bus, and output the converted address to the memory, when the processor performs a memory access for the data having a smaller width than the data bus, and operable to not perform the address conversion when the processor performs a memory access for data having the width of the data bus,

wherein (C) the processor executes a program that defines structure data which includes data that is smaller than a basic word length,

(C1) said structure data being shared between said processor and a first-endian type processor via the memory,

(C2) said data being defined in an order within the basic word length, and

(C3) said order being in reverse to an order in a definition of said structure data in a program to be executed by the first-endian type processor.

According to this configuration, the following three effects (1) to (3) can be produced.

Effect (1): According to the above-mentioned feature (A), the sharing of data having the width of the data bus between said processor and the processor of a different endianness, via the memory, can be implemented with an extremely simple configuration.

Effect (2): According to the above-mentioned features (A) and (B), it becomes possible to access a memory that stores data of a different endianness, for data having a smaller width than the data bus. In addition, since the address conversion unit (B) can be configured through simple hardware, memory access speed is not reduced.

Effect (3): As an effect of the combination of the above-mentioned (B) and (C1) to (C3), it becomes possible to share data of a smaller width than the data bus included in the above-mentioned structure data, between said processor and the processor of a different endianness. In addition, implementation with a simple configuration, and without reducing access speed, becomes possible.

In other words, said processor and the first-endian type processor directly designate mismatched (crisscrossed) addresses for data with a smaller width than the data bus, thereby enabling the sharing of the same data. For example, the address of byte data "a" is seen by said processor as the address "0", and seen by the first-endian type processor as the address "3". The direct designation of mismatched addresses for the same data by said processor and the first-endian type processor is an inevitable consequence of (C2).

To be more specific, see the disclosure in: FIG. 10B; FIG. 11B; page 15, line 29 to page 16, line 3; FIG. 13; page 17, lines 14 to 28 of the specification of the present application.

In this manner, said processor and the first-endian type processor can share data with a smaller width than the data bus, through the designation of different addresses. Furthermore, there is no need to perform rewriting so as to transpose the order of data stored in the memory at the time of a memory access, and there is also no need to

transpose the order of data during memory accessing.

The Examiner asserts that claim 3 of the present application is anticipated by reference Lasserre (USP 6,760,829). However, Lasserre merely discloses a configuration that exhibits results similar to features (A) and (B) in claim 3 of the present application, but does not disclose or suggest a configuration which combines features (A), (B), and (C).

The Examiner asserts that feature (C) is disclosed by Lasserre (FIG. 4, column 9, lines 22 to 25). However, this assertion is incorrect. Lasserre (FIG. 4, column 9, lines 22 to 25) merely indicates byte positions (byte lane 0, byte lane 3) held in a register within the processor. There is absolutely no disclosure or suggestion in Lasserre pertaining to structure data defined within a program.

In FIG. 4 of Lasserre, although it is conceivable that the CPU 402 and the DSP 400 can share data with the same width as the data bus, data with a smaller width than the data bus cannot be easily shared (hereafter referred to as problem I). This is because Lasserre discloses that offsetting from the MSB-end, that is, positioning of data on the data bus is required in order to share data with a smaller width than the data bus (column 9, lines 25 to 29).

In addition, Lasserre discloses two solutions for solving problem I.

For the first solution, Lasserre discloses solving problem I by adding a data positioning function to the MMU and TLB which convert logical addresses to physical addresses (column 9, lines 30 to 34).

For the second solution, Lasserre discloses the rewriting of a memory region when an endianism mismatch occurs in a memory access (FIG. 6; column 10, lines 34 to 38).

In the first solution, the point of requiring special hardware (provided in the MMU, in the reference) for performing the positioning of data presents the problem in that the circuitry becomes complex and circuit size increases (hereafter referred to as problem II).

In the second solution, since a memory region is rewritten though a software routine when an endian mismatch occurs, there is the problem of significant delay time arising in the memory access (hereafter referred to as problem III).

In contrast, although the point of solving problem I is common between the invention recited in claim 3 of the present application and Lasserre, the invention recited in claim 3 solves problem II and problem III which are inherent in Lasserre, through the simple configuration of feature (C) discussed above. More specifically, both the first and second solutions in Lasserre represent the idea of solving problem I at the point when a memory access occurs during the execution of a program, whereas the invention recited in claim 3 of the present application also solves problem II and problem III together with the solution of problem I, not at time when a memory access occurs, but using an approach which is different from that in Lasserre.

In other words, in the invention recited in claim 3 of the present application, the structure data in features (C1) to (C3) discussed above is already defined within the program. Accordingly, since direct access is performed by processors of different endianness using different addresses when memory access occurs, the need for positioning of data at the time when memory access occurs is eliminated. In this manner, in the invention recited in claim 3, problem I as well as problem II and problem III are also previously solved by the time memory access occurs during the execution of the program.

As described thus far, the invention recited in claim 3 solves problem I and problem III which cannot be solved by Lasserre, and produces an effect that cannot be obtained through Lasserre, that is, the effect of realizing the sharing of data with a smaller width than the data bus, without reducing access speed, and using a simple configuration.

Since Lasserre neither discloses nor suggests the addition of feature (C) to features (A) and (B), and an effect which cannot be expected from the reference is produced, claim 3 of the present application is not anticipated by, or obvious in view of, Lasserre.

Independent claims 9, 16, and 19 of the present application also include recitations directed to the aforementioned feature (C), they should also be patentable for the same reasons set forth above with respect to claim 3.

Because of the distinctions discussed above, it is submitted that all of the pending claims, i.e., claims 3, 4, 9-11, 16-19, 21, 22, and 24-27 are allowable over the prior art of record. Accordingly, it submitted that the present application is in condition for

allowance. The Examiner is invited to contact the undersigned by telephone to resolve any remaining issues.

Respectfully submitted,

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